REMARKS

This is in response to the Office Action of 04 November 2003. Claims 1-20 are pending in the application; and Claims 1-20 have been rejected.

Claim 10 has been cancelled; Claims 1, 7, 13-14, and 17-20 have been amended; and Claim 21 has been added.

No new matter has been added.

Applicants respectfully request that these amendments be entered. In view of the amendments above and remarks below, Applicants respectfully request reconsideration and further examination.

About The Invention

The present invention relates generally capacitor structures suitable for use in integrated circuits, and compatible with semiconductor manufacturing processes. The present invention relates more particularly to capacitor structures for integrated circuits, which capacitor structures include a plurality of parallel conductive screen, or mesh, plates, where the plates are substantially perpendicular to the substrate of an integrated circuit, and where alternate plates are electrically coupled to opposite terminals of the capacitor formed by the plurality of screen plates. Each screen, or mesh, structure that makes up the interdigitated elements of the capacitor structure includes what may be viewed as a plurality of beams and a plurality of columns. The beams include vertically stacked, spaced apart, horizontally oriented, conductive lines. Each column includes vertically aligned vias electrically connecting each of the stacked beams to each other. Only dielectric material is disposed between the vertically oriented, interdigitated plates of the capacitor structure. The dielectric material also occupies the openings, or spaces, of the screen-like capacitor plates. By adding vias to each coplanar stack of conductive lines, the effective surface area of each vertically oriented parallel capacitor plate is increased by the surface area of the sidewalls of the vias.

Drawings

The Examiner has approved the drawings that were received on 20 August 2003.

Non-Narrowing Amendment of Claims 17 and 20

Claim 17 has been amended in a non-narrowing manner to correct a grammatical error. Claim 20 has been amended so that it depends from independent Claim 18 rather than dependent Claim 17.

Rejections under 35 USC 103(a)

Claims 1-20 have been rejected under 35 USC 103(a), as being unpatentable over Ng, et al., (US Patent 5.583,359).

Claim 10 has been cancelled.

Independent Claims 1, 13, and 18 have been amended to more clearly distinguish the present invention from the disclosure of Ng, et al. Independent Claim 1 has been amended to expressly recite that the first plane is disposed above a substrate; that the coplanar line pairs are parallel to and extend vertically upward from the substrate; that the lines and the vias which connect them form vertically oriented parallel capacitor plates which are spaced apart from each other and that only dielectric material is disposed between each of the vertically oriented parallel plates. Independent Claim 13 has been amended to expressly recite that the lines and vias form vertically oriented screen structures, each screen structure having dielectric filled openings therein and only dielectric is disposed between the vertically oriented screen structures. Independent Claim 18 has been amended expressly recite that the dielectric layer is disposed between portions of the first and second levels of conductive lines, is also

disposed on the first level adjacent the parallel lines of the first level, and is further disposed on the second level adjacent the parallel lines of the second level; and that the plate structures formed by the lines and vias, are spaced apart from each other, with only the dielectric disposed between each of the plate structures. Additionally, Claim 7 has been amended to recite that each vertically oriented parallel capacitor plate comprises a mesh structure. Claim 14 has been amended so that its language is consistent with its amended base Claim 13. Claim 19 has been amended to recite that the second dielectric layer is disposed between portions of the second and third levels of conductive lines, and is further disposed on the third level adjacent the parallel lines of the third level. Support for these amendments can generally be found throughout the specification and can more particularly be found in Figs. 2B and 2C.

Ng, et al., disclose interdigitated, multi-level capacitor structures. Applicants respectfully submit that Ng, et al., do not disclose the vertically oriented parallel plate structures, which resemble screens or meshes, wherein only dielectric material is disposed between these plates. Applicants further submit that Ng, et al., do not suggest the inventive structure set forth in Applicants' amended Claims.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the rejections of Claims 1-9 and 11-20 have been overcome.

New Claim 21

New Claim 21 depends from amended Claim 19, and recites that each of the at least four plate structures form a screen with the dielectric disposed in the openings of the screen; the plate structures extend vertically upward from a substrate and are perpendicular to the substrate. Ng, et al., does not disclose or suggest such a capacitor structure. Support for Claim 21 can generally be found throughout the specification and can more particularly be found in Fig. 2B.

Conclusion

All of the rejections in the outstanding Office Action of 04 November 2003 have been responded to, and Applicants respectfully submit that the pending Claims 1-9 and 11-21 are now in condition for allowance.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

By Raymond J. Werner

Dated: 24 December 2003
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